Boot Time Configuration

Name	Chip	Pin	Signal	Pol	Enable	Disable	Description
Serial Enable	U19	AA04	VGPIO1	L	JP1	**R58**	OFW disables camera port and enables the main processor serial port when enabled at boot time.
Memory ID	U19	AL10	GPIO9	H	R89	**R90**	When enabled (H), select a CL value of 4 (800MHz DDR2 memory chip). When disabled (L), use a CL value of 3 (600 MHz DDR2 memory chip).
Mem Bus Width (MEM ID 1)	U19	AF10	GPIO14	H	R94	**R95**	When enabled (H), selects a 32b memory bus (four DRAM chips). When disabled (L), selects a 64b memory bus (eight DRAM chips).
DCON on CRT I2C	U17	126	DCONSDATA		**R273**	R228	When enabled, the DCON control bus is driven by the VX855 CRT I2C. When disabled, it is driven by the VX855 GPIO0/1.
		128	DCONSCLK		**R272**	R232	
DCON Display Control	PR114	1	DBC		**R221**	R42	When enabled, the DCON controls these signals. When disabled, they are controlled by the VX855.
	PU11	4	BACKLIGHT		**R219**	R37	
	PU9	4	VDDEN		**R223**	R47	
	PQ19	2	VGH_EN		**R222**	R50	
CPU Frequency	U22	1	FSLA	H	**R302**	R304	Using [FSLA, FSLB, FSLC], the values are 000 => 266 MHz, 001 => 333 MHz, 010 => 200 MHz, 011 => 400 MHz, 100 => 133 MHz, **101 => 100 MHz**, 110 => 166 MHz, 111 => 200 MHz. Only allowed values on CL1B are 101 (100 MHz) and 111 (200 MHz).
		6	FSLB	H	R317	**R316**	
		12	FSLC	H	**R333**	R329	
FSB Frequency	U19	AM11	GPIO10	H	**R361**	R363	Using GPIO[12, 11, 10], acceptable values are: 000 => 100 MHz, 001 => 133 MHz, 010 => 200 MHz, 011 => 266 MHz, **111 => Auto mode**. Other values are reserved.
		AL11	GPIO11	H	**R358**	R355	
		AJ09	GPIO12	H	**R263**	R264	
VX855 Debug Mode	U19	J19	TP2	H	R25	**R27**	Enables VX855 Debug mode
GTL Pull up	U19	AK10	GPIO13	L	**R267**	R266	GTL pullups enabled when low
IOQ Depth	U19	AH03	PDA0	L	**R46**	R35	Enables an IOQ depth of 12 when low
PLL OK Source	U19	AH04	PDA1	H	**R45**		Enable OK from logic ctr. Always enabled
Debug Mode	U19	AJ10	SPKR/GPO0	H	R86	**R87**	Enables VX855 debug mode on reset
SPI/LPC ROM	U19	AG10	AZBITCLK	H		**R82**	Disable (L) selects LPC boot ROM. Enable (H) selects SPI Boot ROM.
System Auto Reboot	U19	AF09	AZSDOUT	L	R73	**R72**	Enable VX855 watchdog reset when pulled low
LPC FWH Command	U19	AJ07	AZSYNC	L	**R78**	R77	Enable use of FWH commands when pulled low
IDE Controller	U19	AM06	MSPISS1	H		**R270**	Using [MSPISS1, MSPISS0], **00 => IDE**, 01 => NFC ROM, 10 => CE ATA. Other values reserved
		AK06	MSPISS0	H		**R54**	
Boot ROM I/F	U19	AJ08	MSPISS2	H		**R83**	Always low for SPI/LPC ROM
Debug Link	U19	AK08	TDO	H		**R269**	Pull low to disable Debug, enable SDIO2
PCI Master Mode	U19	AJ03	PDA2	H		**R34**	
DVP1TVCLKR	U19	Y1	GFRDATA4	L	R67		Via request
Required	U19	AD06	PIXDATA7	L	**R69**		VX855 datasheet requires this
	U19	AC05	-	L	**R75**		
	U19	AD03	-	L	**R84**		
	U19	M28	CKEA0	L	**R152**		VX855 errata requires this

These are boot options specified by the chip manufacturers. Additional boot options specified by software are specified in the GPIO mapping.

"Pol" indicates the polarity of the boot option. If H, the option is enable when pulled to a high voltage. If L, the option is enabled by pulling to a low voltage. If blank, the option switches between two signal sources.

Enable or Disable resistors indicated in bold are those which are currently populated.